AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently amended) A multiple-layer diffusion junction capacitor structure comprising:

an N-type region formed in a semiconductor substrate and having an N-type vertical portion and a plurality of spaced-apart N-type fingers that extend from the N-type vertical portion; and

a P-type region formed in a semiconductor substrate and having a P-type vertical portion and a plurality of spaced-apart P-type fingers that extend from the P-type vertical portion, and

wherein the N-type fingers and the P-type fingers are inter-digitated and in direct contact.

2. (Currently amended) A multiple-layer diffusion junction capacitor structure as in claim 1, and further comprising:

a first conductive [contact] electrode formed on an upper surface of the N-type region; and

a second conductive electrode formed on an upper surface of the P-type region.

3. (Original) A multiple-layer diffusion junction capacitor structure as in claim 2, and wherein both the first conductive electrode and the second conductive electrode comprise aluminum.

4. (Original) A method of forming an N-layer junction capacitor structure in a semiconductor substrate, wherein N is an integer, the method comprising:

forming a patterned mask on an upper surface of the semiconductor substrate, the patterned mask having at least one opening formed therein to expose an upper surface area of the semiconductor substrate;

forming a sequence of N alternating implants of P-type dopant and of N-type dopant at negative and positive implant angles, respectively, for a particular conductivity type dopant each implant being performed with a different energy and implant dose, thereby resulting in N inter-digitated layers of P-type dopant and N-type dopant formed in a semiconductor substrate; and

forming a first conductive electrode in electrical contact with the P-type dopant layers and a second conductive electrode in electrical contact with the N-type dopant layers.

5. (Original) A method as in claim 4, and wherein the patterned mask comprises silicon oxide.

6. (Currently amended) A method as in claim 4, and wherein the first and second conductive electrodes comprise [alumimun] aluminum.